WHAT IS CLAIMED IS:

1. A processor having a plurality of processor functions for executing each of a plurality of instruction sets, comprising:

a system instruction decoder, provided separately of the plurality of processor functions, for decoding a system instruction that is not executed by any of the plurality of processor functions; and

a system instruction execution unit for selecting one of the plurality of processor functions in response to said system instruction decoded by said system instruction decoder.

2. The processor according to claim 1, wherein said system instruction execution unit selects one of the plurality of processor functions in response to a prescribed interrupt signal.

3. The processor according to claim 1, wherein at least two of the plurality of processor functions share hardware resources.

4. The processor according to claim 1, wherein at least two of the plurality of instruction sets include a common instruction, and a plurality of processor functions corresponding to said at least two instruction sets share an instruction set decoder for decoding the common instruction.

5. The processor according to claim 1, wherein the system instruction includes at least one instruction that sets power-supply voltage and operating speed at which the processor operates.

6. The processor according to claim 1, further comprising a storage unit for storing processing control data corresponding to each instruction included in the plurality of instruction sets;

wherein on the basis of an entered instruction and information regarding a selected processor function, an address that corresponds to the entered instruction is generated and processing control data corresponding to the entered instruction is read out of said storage unit.

7. The processor according to claim 1, wherein at least two processor functions among the plurality thereof have a common instruction set.

8. The processor according to claim 1, wherein at least one processor function among the plurality thereof undergoes pipeline control in which number of stages thereof is set variably, and the number of stages in the pipeline control is set in response to a predetermined system instruction.

9. A processor having a pipeline control architecture, said processor comprising:

a unit for receiving a stage-number setting instruction; and

a unit for setting variably the number of stages in the pipeline control in response to the received stage-number setting instruction.

10. A system LSI circuit having the processor set forth in claim 1.

11. A system LSI circuit having a plurality of the processors set forth in claim 1.

12. The system LSI circuit according to claim 11, wherein the plurality of processors operate based upon either a first pattern in which all processors operate according to the same instruction set, or a second pattern in which at least one processor operates according to an instruction set that is different from those of the other processors.

13. A method of designing a system LSI circuit having a plurality of processors each having a plurality of processor functions for executing a

plurality of instruction sets, said method comprising the steps of:

(a) dividing system LSI circuit design specifications into hardware design and software design at a function designing stage;

(b) receiving, as hardware information in hardware design, hardware configurations corresponding to respective ones of the plurality of processors, and the system instruction and the plurality of instruction sets described at an algorithm level; and

(c) performing behavioral synthesis using the hardware information.

14. The method according to claim 13, wherein said processor includes:

a system instruction decoder, provided separately of the plurality of processor functions, for decoding a system instruction that is not executed by any of the plurality of processor functions; and

a system instruction execution unit for selecting one of the plurality of processor functions in response to the system instruction decoded by said system instruction decoder.

15. The method according to claim 13, wherein an HDL description for logic synthesis, a simulation description and synthesis information indicating size of the hardware are generated at said behavioral synthesis step (c).

16. The method according to claim 15, further comprising the step

(d) verifying operation of a system LSI circuit, which is to be designed, based upon the simulation description and a machine language instruction of software that operates the plurality of processors, the step

(d) following said behavioral synthesis step (c).

17. The method according to claim 16, wherein it is determined whether to return to the dividing step (a) based upon the synthesis information and the result of verification performed at the verifying operation step (d).

18. The method according to claim 13, further comprising the steps of:

(e) creating a source program, which includes instructions of the plurality of instruction sets and a system instruction, for each of the plurality of processors at designing of the software; and

(f) translating the source programs of every processor into machine language collectively by referring to the hardware information.

19. A computer-readable recording medium on which is recorded a program for causing a computer to execute designing a system LSI circuit having a plurality of processor functions for executing a plurality of instruction sets, said program comprising the processes of:

(a) dividing system LSI circuit design specifications into hardware design and software design at a function designing stage;

(b) receiving, in hardware design, as hardware information, hardware configurations corresponding to respective ones of the plurality of processors, and the system instruction and the plurality of instruction sets described at an algorithm level; and

(c) performing behavioral synthesis using the hardware information.

20. The computer-readable recording medium according to claim 19, wherein said processor includes:

a system instruction decoder, provided separately of the plurality of processor functions, for decoding a system instruction that is not executed by any of the plurality of processor functions; and

a system instruction execution unit for selecting one of the plurality of processor functions in response to the system instruction decoded by said system instruction decoder.

21. A processor apparatus comprising:

an instruction fetch register for storing an instruction fetched;

a plurality of instruction decoders, each receiving and decoding an instruction of an instruction set associated with said instruction decoder;

a plurality of instruction execution controllers, each being provided in association with the corresponding instruction decoder, for receiving a decoded result of the instruction by the corresponding instruction decoder for controlling the execution of the instruction;

an instruction set change over unit for selecting at least one among the plurality of instruction decoders and for supplying an instruction output from said instruction fetch register to the selected instruction decoder;

a system instruction decoder receiving a predetermined system instruction from instruction fetch register for decoding the predetermined system instruction; and

a system instruction execution controller receiving the decoded result from said system instruction decoder; said system instruction execution controller controlling said instruction set change over unit to

change over the selection of the plurality of instruction decoders, in accordance with said system instruction decoded by said system instruction decoder, in case said system instruction being an instruction specifying the instruction set to be used among a plurality of instruction sets.

22. The processor apparatus according to claim 21, wherein said system instruction execution controller performs control to dynamically change over the number of stages in a pipeline from an instruction fetch stage to an instruction execution stage for an instruction set being used, in accordance with said system instruction decoded by said system instruction decoder, in case said system instruction being an instruction that specifies the number of pipeline stages for the instruction set.